Freescale Semiconductor
Addendum

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Errata to Symphony™ DSP56724/DSP56725 Multi-Core Audio Processors Reference Manual, Rev. 0

This errata describes corrections to the *DSP56724/DSP56725 Multi-Core Audio Processors Reference Manual*, Revision 0. For convenience, the section number and page number of the errata item in the reference manual are provided.

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Section, Page No.	Changes
Throughout	Remove all references to HD.
About This Book	Modify the second paragraph, as follows: "The DSP56724/DSP56725 Multi-Core Audio Processors are devices of the DSP5672x family of programmable CMOS DSPs, designed using dual DSP56300 24-bit cores. The DSP56724/DSP56725 are intended for automotive, consumer, and professional audio applications that require high performance for audio processing. Potential applications include A/V receivers, car audio/amplifiers, and professional audio equipment."
1.1/1-1	In the list of features, change "400 MIPs (200 MIPs/core) with a 200 MHz clock" to say "up to 500 MIPs (up to 250 MIPs/core) with up to 250-MHz clock..."
1.4.2/1-5	Modify the second sentence in the first paragraph, as follows: "The DSP56724/DSP56725 shared memory has four 8-Kword × 24-word memory blocks for a total of 32-Kword shared words and is located starting from $030000."
1.4.5/1-6	Revise section, as follows: "Each Triple Timer is composed of a common 21-bit prescaler and three independent and identical general purpose 24-bit timer event counters, with each timer having its own register set. Each timer uses internal clocking, and can also interrupt the DSP after a specified number of events (clocks). Each timer can also be used to trigger DMA transfers after a specified number of events (clocks) have occurred."
2.2.9/2-13	In Table 2-13, "Enhanced Serial Audio Interface Signals (ESAI_2)," change all instances of the following sentence: "Uses internal pull-up resistor in DSP56725 80-pin and 144-pin packages" to: "Uses internal pull-up resistor in DSP56725 80-pin package."
2.2.12/2-28	In Table 2-19, "Digital Audio Interface: S/PDIF Signals," remove both instances of the following sentence: "This pin is only available in the DSP56724 and DSP56725 144-pin package."
3.1/3-1	Change the sentence "Four blocks of 8 Kbytes" to say "Eight blocks of 4 Kwords."
3.2/3-3	Switch Table 3-1 and Table 3-2, change the title of Table 3-1 to "Core-0 Configuration," and change the title of Table 3-2 to "Core-1 Configuration." In addition, switch Table 3-3 and Table 3-4, change the title of Table 3-3 to "DSP Core-0 Memory Map Locations," and change the title of Table 3-4 to "DSP Core-1 Memory Map Locations."
3.2/3-3	In Table 3-4, "DSP Core-1 Memory Map Locations," for MSW = NA, MS = 0, change program RAM range from "$000000–$007FFF" to "$000000–$0007FF."
4.2/4-2	In list of features, change second bullet to: "Up to 250 million instructions per second (MIPS) with up to 250-MHz clock with 1.2-V internal logic supply"

Section, Page No.	Changes
7.1.1/7-1	Change 200 MHz to 250 MHz, and 400 MHz to 500 MHz.
7.3.3.2/7-10	Add new row to the top of Table 7-9, “PLL Programming Examples,” as follows:

Table 7-9. PLL Programming Examples

Extal (MHz)	NR (= R + 1)	Fref (= Fosc/NR) (2~8 MHz)	NF (= F + 1)	Fvco (= Fref*NF) (200~400 MHz)	NO (=2^OD)	PLL Output (= Fvco/NO) (MHz)	PLL Setting (0x)
24.576	12	2.048	122	249.856	1	249.856	2B2079

8.2.6/8-10	Remove the following sentence: “When not used as timer signals, the two sets of timer event counter signals (TIO0, TIO1, TIO2, TIO0_1, TIO1_1, TIO2_1) can be configured as GPIO signals.”
11.1.1/11-1	Modify the first and second bullet, as follows: • Uses internal clocking. • Interrupts the DSP Core after a specified number of events (clocks)
Chapter 12	Remove Chapter 12, “Host Data Interface (HDI24, HDI24_1).”
12.2/12-1	Change first sentence of second paragraph to: “In the DSP56725 (80-pin package) and the DSP56724 (144-pin package), the WDT and WDT_1 pins are ‘ORed’ together, so that when either watchdog timer times out, the external pin is asserted.”
15.1/15-1	Change memory space address to “$030000–$37ffff.” In addition, change “4 × 8 Kbytes” to “8 × 4 Kwords,” and change “Multiples of 8K memory blocks...” to “Consists of multiple 4-Kword memory blocks...”
19.1.2/19-3	In Table 19-1, “ASRC Specifications,” add the following note to 40 ms: “The settling time is defined to be the time from audio input to the conversion performance reaching –115 dB THD + N.”
19.1.2/19-3	Add two new bullets, as follows: • Output sampling rates in the range of 8 kHz to 200 kHz are also supported but with less performance. • Designed for real-time streaming audio usage i.e. the output sampling clock must always be physically available in the system.
19.1.2/19-3	Significantly revise the first bullet under “Clock/Data Connections,” as follows: • The physical sampling clocks are directly connected to the ASRC module and the ratio estimation of the input clocks with output clocks are done in ASRC hardware when both the input and output sampling clocks are physically available. When this is the case, the rate conversion can be done by configuring the physical clocks.
19.1.2/19-3	Modify last sub-bullet, as follows: “Core master clock derivative (default is 5.644 MHz, programmable through external module)”
19.1.3.1/19-4	Change headings of modes 1–3 to be more specific, as follows:

Section, Page No.	Changes

- “Data Input Mode 1 (Polling Mode)”
- “Data Input Mode 2 (Interrupt Mode)”
- “Data Input Mode 3 (DMA Mode)”
- “Data Output Mode 1 (Polling Mode)”
- “Data Output Mode 2 (Interrupt Mode)”
- “Data Output Mode 3 (DMA Mode)”

Data Input Mode 1 (Polling Mode)/19-4 — Add the following text: “the FIFO size of each channel is 64 samples.”

Data Output Mode 1 (Polling Mode)/19-5 — Add the following text: “the FIFO size of each channel is 64 samples.”

19.2/19-5 — In Table 19-2, “Block Memory Map,” changed rows for 0xC, 0xD, and 0xF to reserved and added new rows for new registers. 19.2.2.1/19-8Modify Figure 19-4, “ASRC Control Register (ASRCTR),” and Table 19-4, “ASRC Control Register Bits (ASRCTR),” as follows:

Offset 0x0 Access: Mixed

	23	22	21	20	19	18	17	16	15	14	13	12
R W	ASDBG	ATSC	ATSB	ATSA	—	USRC	IDRC	USRB	IDRB	USRA	IDRA	—
Reset	All zeros											

	11	5	4	3	2	1	0
R W	—		SRST	ASREC	ASREB	ASREA	ASRCEN
Reset	All zeros						

Figure 0-4. ASRC Control Register (ASRCTR)

Table 0-4. ASRC Control Register Bits (ASRCTR)

Bit	Field	Description
23	ASDBG	ASRC Debug Control Enable ASRC to enter debug mode.
22	ATSC	ASRC Pair C Automatic Selection For Processing Options When the ASTC bit is 1, pair C will automatic update its pre-processing and post-processing options (ASRCFG: PREMODC, ASRCFG:POSTMODC; see Section 19.2.2.4, “Filter Configuration Status Register (ASRCFG)”) based on the frequencies it detected. To use this option, the two parameter registers (TS76KHZ and TS56KHZ) should be set correctly (see Section 19.2.2.12.4, “ASRC 76 kHz Period Register in Terms of Master Clock (ASR76K)”). This bit should be disabled when {USRC, IDRC}={1,1}.

Table 0-4. ASRC Control Register Bits (ASRCTR) (continued)

Bit	Field	Description
21	ATSB	ASRC Pair B Automatic Selection For Processing Options When the ATSB bit is 1, pair B will automatic update its pre-processing and post-processing options (ASRCFG: PREMODB, ASRCFG:POSTMODB; see Section 19.2.2.4, “Filter Configuration Status Register (ASRCFG)”) based on the frequencies it detected. To use this option, the two parameter registers (ASR76K and ASR56K) should be set correctly (see Section 19.2.2.12.4, “ASRC 76 kHz Period Register in Terms of Master Clock (ASR76K)”). When the ATSB bit is 0, the user is responsible for choosing the proper processing options for pair B. This bit should be disabled when {USRB, IDRB}={1,1}.
20	ATSA	ASRC Pair A Automatic Selection For Processing Options When the ATSA bit is 1, pair A will automatic update its pre-processing and post-processing options (ASRCFG: PREMODA, ASRCFG:POSTMODA; see Section 19.2.2.4, “Filter Configuration Status Register (ASRCFG)”) based on the frequencies it detected. To use this option, the two parameter registers (ASR76K and ASR56K) should be set correctly (see Section 19.2.2.12.4, “ASRC 76 kHz Period Register in Terms of Master Clock (ASR76K)”). When the ATSA bit is 0, the user is responsible for choosing the proper processing options for pair A. This bit should be disabled when {USRA, IDRA}={1,1}.
19	—	Reserved
18	USRC	Use Ratio for Pair C Use ratio as the input to ASRC. This bit is used in conjunction with IDRC control bit.
17	IDRC	Use Ideal Ratio for Pair C When USRC=0, this bit has no usage. When USRC=1 and IDRC=0, ASRC internal measured ratio will be used. When USRC=1 and IDRC=1, idea ratio from the interface register ASRIDRHC, ASRIDRLC will be used. It issuggested to manually set ASRCFG:POSTMODC, ASRCFG:PREMODC
16	USRB	Use Ratio for Pair B Use ratio as the input to ASRC. This bit is used in conjunction with IDRB control bit.
15	IDRB	Use Ideal Ratio for Pair B When USRB=0, this bit has no usage. When USRB=1 and IDRB=0, ASRC internal measured ratio will be used. When USRB=1 and IDRB=1, idea ratio from the interface register ASRIDRHB, ASRIDRLB will be used.It is suggested to manually set ASRCFG:POSTMODB, ASRCFG:PREMODB.
14	USRA	Use Ratio for Pair A Use ratio as the input to ASRC. This bit is used in conjunction with IDRA control bit.
13	IDRA	Use Ideal Ratio for Pair A When USRA=0, this bit has no usage. When USRA=1 and IDRA=0, ASRC internal measured ratio will be used. When USRA=1 and IDRA=1, idea ratio from the interface register ASRIDRHA, ASRIDRLA will be used. It is suggested to manuallymanually set ASRCFG:POSTMODA, ASRCFG:PREMODA.
12–5	—	Reserved
4	SRST	Software Reset This bit is self-clear bit. Once it is been written as 1, it will generate a software reset signal inside ASRC. After 9 cycles of the master clock, this reset process will stop, and this bit will be cleared automatically.
3	ASREC	ASRC Enable C Enables the conversion of pair C of the ASRC. When ASREC is cleared, conversion of pair C is disabled.

Table 0-4. ASRC Control Register Bits (ASRCTR) (continued)

Bit	Field	Description
2	ASREB	ASRC Enable B Enables the conversion of pair B of the ASRC. When ASREB is cleared, conversion of pair B is disabled.
1	ASREA	ASRC Enable A Enables the conversion of pair A of the ASRC. When ASREA is cleared, conversion of pair A is disabled.
0	ASRCEN	ASRC Enable Enables the operation of the ASRC.

19.2.2.9/19-23 Remove section, “Memory Access Registers (ASRMAA, ASRMAD).”

19.2.2.12/19-26 Add Section 19.2.2.12.1, “Ideal Ratio Registers for Pair A, High/Low Part (ASRIDRHA, ASRIDRLA),” through Section 19.2.2.12.5, “ASRC 56 kHz Period Register in Terms of Master Clock (ASR56K),” as follows:

0.2.2.12.1 Ideal Ratio Registers for Pair A, High/Low Part (ASRIDRHA, ASRIDRLA)

These are three 24-bit wide register for reading data from the output data FIFOs Ideal Ratio Registers for Pair A, High/Low Part (ASRIDRHA, ASRIDRLA) The ideal ratio registers (ASRIDRHA, ASRIDRLA) hold the ratio value IDRATIOA. IDRATIOA = $Fs_{inA}/Fs_{outA} = Ts_{outA}/Ts_{inA}$ is a 32-bit fixed point value with 26 fractional bits. This value is only useful when ASRCTR:{USRA, IDRA}=2’b11.

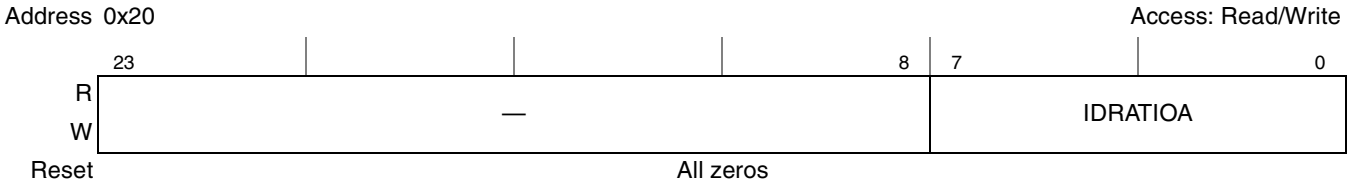

Figure 0-15. Ideal Ratio Register for Pair A, High Part (ASRIDRHA)

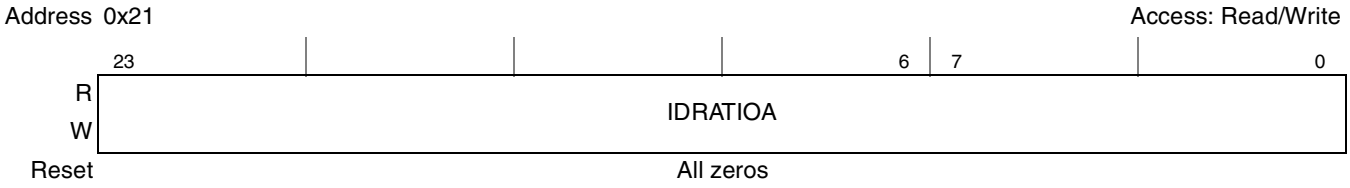

Figure 0-16. Ideal Ratio Register for Pair A, Low Part (ASRIDRLA

0.2.2.12.2 Ideal Ratio Registers for Pair B, High/Low Part (ASRIDRHB, ASRIDRLB)

The ideal ratio registers (ASRIDRHB, ASRIDRLB) hold the ratio value IDRATIOB. IDRATIOB = $Fs_{inB}/Fs_{outB} = Ts_{outB}/Ts_{inB}$ is a 32-bit fixed point value with 26 fractional bits. This value is only useful when ASRCTR:{USRB, IDRB}=2’b11.

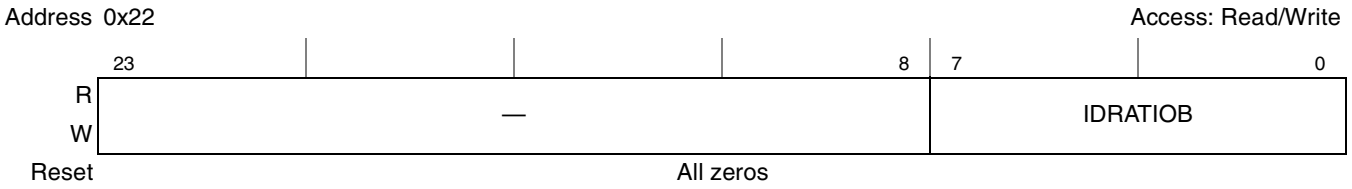

Figure 0-17. Ideal Ratio Register for Pair B, High Part (ASRIDRHB)

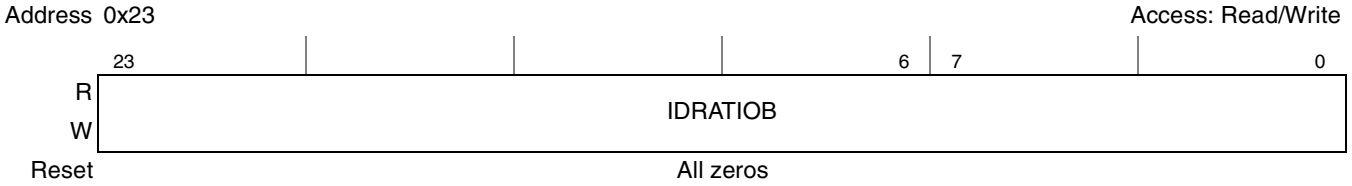

Figure 0-18. Ideal Ratio Register for Pair B, Low Part (ASRIDRLB)

0.2.2.12.3 Ideal Ratio Registers for Pair C, High/Low Part (ASRIDRHC, ASRIDRLC)

The ideal ratio registers (ASRIDRHC, ASRIDRLC) hold the ratio value IDRATIOC. IDRATIOC = $Fs_{inC}/Fs_{outC} = Ts_{outC}/Ts_{inC}$ is a 32-bit fixed point value with 26 fractional bits. This value is only useful when ASRCTR:{USRC, IDRC}=2'b11.

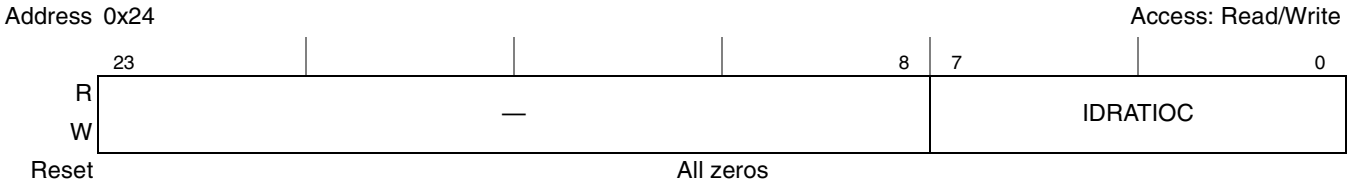

Figure 0-19. Ideal Ratio Register for Pair C, High Part (ASRIDRHC)

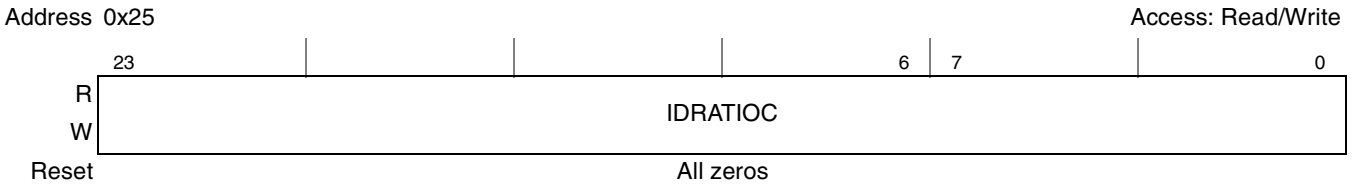

Figure 0-20. Ideal Ratio Register for Pair C, Low Part (ASRIDRLC)

0.2.2.12.4 ASRC 76 kHz Period Register in Terms of Master Clock (ASR76K)

The register (ASR76K) holds the period of the 76 kHz sampling clock in terms of the master clock. ASR76K = Fs_{master}/Fs_{76k}. Reset value is $0A47 which assumes that Fs_{master}=200 MHz. This register is used to help the ASRC internal logic to decide the pre-processing and the post-processing options automatically (see Section 19.2.2.1, "ASRC Control Register (ASRCTR)," and Section 19.2.2.4, "Filter Configuration Status Register (ASRCFG)").

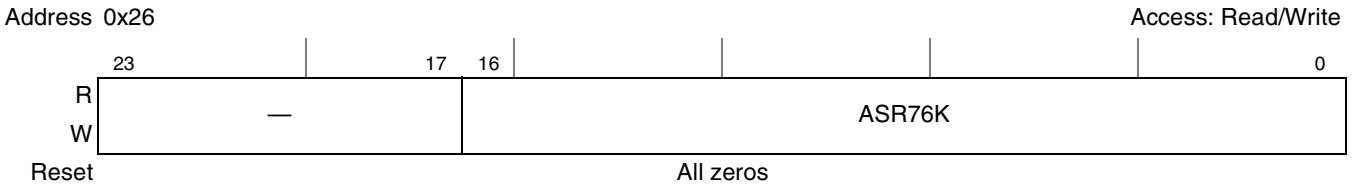

Figure 0-21. ASRC 76 kHz Period Register (ASR76K)

0.2.2.12.5 ASRC 56 kHz Period Register in Terms of Master Clock (ASR56K)

The register (ASR56K) holds the period of the 56 kHz sampling clock in terms of the master clock. ASR56K = Fs_{master}/Fs_{56k}. Reset value is $0DF3 which assumes that Fs_{master}=200 MHz. This register is used to help the ASRC internal logic to decide the pre-processing and the post-processing options automatically (ssee Section 19.2.2.1, “ASRC Control Register (ASRCTR),” and Section 19.2.2.4, “Filter Configuration Status Register (ASRCFG)”).

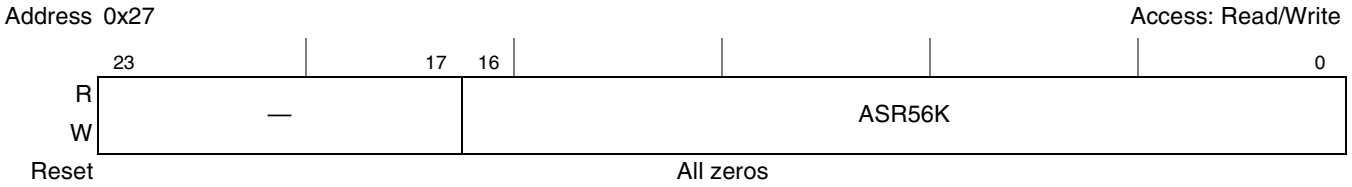

Figure 0-22. ASRC 56kHz Period Register (ASR56K

19.2.2.4/19-12 Change bit 20 from reserved to “NDPRC” in Figure 19-8, “Filter Configuration Status Register (ASRCFG),” and Table 19-8, “Filter Configuration Status Register (ASRCFG),” as follows:

“Not Use Default Parameters for RAM-stored Parameters For Conversion Pair C

0 Use default parameters for RAM-stored parameters. Override any parameters already in RAM.

1 Do not use default parameters for RAM-stored parameters. Use the parameters already stored in RAM.”

19.2.2.5/19-15 Add values 1000–1100 to each bit field description in Table 19-9, “Clock Source Register (ASRCSR),” as follows:

Table 0-9. Clock Source Register (ASRCSR)

Bit	Field	Description
23–20	AOCSC	Output Clock Source C 0000 ESAI Tx clock 0001 ESAI-1 Tx clock 0010 ESAI-2 Tx clock 0011 ESAI-3 Tx clock 0100 S/PDIF Tx clock 0101 Reserved 0110 Reserved 0111 Reserved 1000 ESAI Rx clock 1001 ESAI-1 Rx clock 1010 ESAI-2 Rx clock 1011 ESAI-3 Rx clock 1100 SPDIF Rx clock Any other value—ASRCK1 (In DSP56724/DSP56725, this signal is derived from the PLL, and can be controlled by the ASCDR register in the CGM module.)
19–16	AOCSB	Output Clock Source B 0000 ESAI Tx clock 0001 ESAI-1 Tx clock 0010 ESAI-2 Tx clock 0011 ESAI-3 Tx clock 0100 S/PDIF Tx clock 0101 Reserved 0110 Reserved 0111 Reserved 1000 ESAI Rx clock 1001 ESAI-1 Rx clock 1010 ESAI-2 Rx clock 1011 ESAI-3 Rx clock 1100 SPDIF Rx clock Any other value—ASRCK1 (In DSP56724/DSP56725, this signal is derived from the PLL, and can be controlled by the ASCDR register in the CGM module.)
15–12	AOCSA	Output Clock Source A 0000 ESAI Tx clock 0001 ESAI-1 Tx clock 0010 ESAI-2 Tx clock 0011 ESAI-3 Tx clock 0100 S/PDIF Tx clock 0101 Reserved 0110 Reserved 0111 Reserved 1000 ESAI Rx clock 1001 ESAI-1 Rx clock 1010 ESAI-2 Rx clock 1011 ESAI-3 Rx clock 1100 SPDIF Rx clock Any other value—ASRCK1 (In DSP56724/DSP56725, this signal is derived from the PLL, and can be controlled by the ASCDR register in the CGM module.)

Table 0-9. Clock Source Register (ASRCSR) (continued)

Bit	Field	Description
11–8	AICSC	Input Clock Source C 0000 ESAI Rx clock 0001 ESAI-1 Rx clock 0010 ESAI-2 Rx clock 0011 ESAI-3 Rx clock 0100 S/PDIF Rx clock 0101 Reserved 0110 Reserved 1000 ESAI Tx clock 1001 ESAI-1 Tx clock 1010 ESAI-2 Tx clock 1011 ESAI-3 Tx clock 1100 SPDIF Tx clock Any other value—ASRCK1 (In DSP56724/DSP56725, this signal is derived from the PLL, and can be controlled by the ASCDR register in the CGM module.)
7–4	AICSB	Input Clock Source B 0000 ESAI Rx clock 0001 ESAI-1 Rx clock 0010 ESAI-2 Rx clock 0011 ESAI-3 Rx clock 0100 S/PDIF Rx clock 0101 Reserved 0110 Reserved 1000 ESAI Tx clock 1001 ESAI-1 Tx clock 1010 ESAI-2 Tx clock 1011 ESAI-3 Tx clock 1100 SPDIF Tx clock Any other value—ASRCK1 (In DSP56724/DSP56725, this signal is derived from the PLL, and can be controlled by the ASCDR register in the CGM module.)
3–0	AICSA	Input Clock Source A 0000 ESAI Rx clock 0001 ESAI-1 Rx clock 0010 ESAI-2 Rx clock 0011 ESAI-3 Rx clock 0100 S/PDIF Rx clock 0101 Reserved 0110 Reserved 1000 ESAI Tx clock 1001 ESAI-1 Tx clock 1010 ESAI-2 Tx clock 1011 ESAI-3 Tx clock 1100 SPDIF Tx clock Any other value—ASRCK1 (In DSP56724/DSP56725, this signal is derived from the PLL, and can be controlled by the ASCDR register in the CGM module.)

19.2.2.8/19-21 Change title of section to “ASRC Debug Control Register (ASRCDR).”

In addition, remove Figure 19-14, “Debug Control Register-1 (ASRDCR1),” and Table 19-13, “Debug Control Register-1 (ASRDCR1).”

19.5.1.1/19-30 Add new column “8” and new rows “8,” “12,” “16,” and “24,” to Table 19-19, “Pre-Processing, Post-Processing Options,” as follows:

Table 19-19. Pre-Processing, Post-Processing Options

{Pre_Proc, Post_Proc}		Fsout (kHz)								
		8	**32**	**44.1**	**48**	**64**	**88.2**	**96**	**128**	**192**
Fsin (kHz)	**8**	{0, 1}	{0, 0}	{0, 0}	{0, 0}	{0, 0}	{0, 0}	{0, 0}	{0, 0}	{0, 0}
	12	{0, 2}	{0, 1}	{0, 0}	{0, 0}	{0, 0}	{0, 0}	{0, 0}	{0, 0}	{0, 0}
	16	{1, 2}	{0, 1}	{0, 1}	{0, 1}	{0, 0}	{0, 0}	{0, 0}	{0, 0}	{0, 0}
	24	{1, 2}	{0, 1}	{0, 1}	{0, 1}	{0, 1}	{0, 0}	{0, 0}	{0, 0}	{0, 0}
	32	{1, 2}	{0, 1}	{0, 1}	{0, 1}	{0, 1}	{0, 1}	{0, 1}	{0, 0}	{0, 0}
	44.1	{2, 2}	{0, 2}	{0, 1}	{0, 1}	{0, 1}	{0, 1}	{0, 1}	{0, 0}	{0, 0}
	48	{2, 2}	{0, 2}	{0, 2}	{0, 1}	{0, 1}	{0, 1}	{0, 1}	{0, 1}	{0, 0}
	64	{2, 2}	{1, 2}	{0, 2}	{0, 2}	{0, 1}	{0, 1}	{0, 1}	{0, 1}	{0, 0}
	88.2	N/A	{1, 2}	{1, 2}	{1, 2}	{1, 1}	{1, 1}	{1, 1}	{1, 1}	{1, 0}
	96	N/A	{1, 2}	{1, 2}	{1, 2}	{1, 1}	{1, 1}	{1, 1}	{1, 1}	{1, 1}
	128	N/A	{1, 2}	{1, 2}	{1, 2}	{1, 1}	{1, 1}	{1, 1}	{1, 1}	{1, 1}
	192	N/A	{2, 2}	{2, 2}	{2, 2}	{2, 1}	{2, 1}	{2, 1}	{2, 1}	{2, 1}

Comments:
In the {Pre_Proc, Post_Proc} pair, the meaning of the values {x, y}are:
Pre_Proc:
- 0 Pre-processing input path I0 as shown in Figure 19-19
- 1 Pre-processing input path I1 as shown in Figure 19-19
- 2 Pre-processing input path I2 as shown in Figure 19-19
- Post_Proc:
- 0 Post-processing output path O0 as shown in Figure 19-19
- 1 Post-processing output path O1 as shown in Figure 19-19
- 2 Post-processing output path O2 as shown in Figure 19-19

19.5.1.2.1/19-30 Change the only sentence in this section to say, “The device supports only physical sampling clocks. The clocks can be the clocks from SPDIF, ESAI, or the PLL.”

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